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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/605,329	09/23/2003	Yi-Chang Chen	WISP0035USA	2328

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EXAMINER	
SCHNEIDER, JOSHUA D	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 10/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/605,329	CHEN ET AL.	
	Examiner	Art Unit	
	Joshua D. Schneider	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 August 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8 and 24-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-8 and 24-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 8/8/2006 have been fully considered but they are not persuasive. Applicant has argued that Ishii does not teach the first program being executed and copied from the same memory. However, Ishii does teach such an embodiment as show in Figures 8 and 9. The rejections below are changed to show points in the reference that the Applicant may have believed to be distinguishing, but are within the scope of the teaching of the reference. Further, new rejections are set forth for the new claims below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-3, 5, 7, and 8 are rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent 5,835,761 to Ishii et al.

4. With regards to claim 1, Ishii teaches (a) executing the first code in the first storage device (Fig. 8, element C2); (b) after proceeding with step (a), executing an examining process before the first storage device transfers the command to the second storage device (Fig. 8, element C4); (c) after proceeding with step (b), the first storage device transferring the command to the second storage device to operate the computer system when a result of the examining process is correct (Fig. 8, element C5); and (d) after proceeding with step (b), the first storage

device not transferring or failing the command to the second storage device when the result of the examining process is incorrect (Fig. 8, elements C9).

5. With regards to claim 2, Ishii teaches (e) in step (b), examining whether a predetermined instruction of the second code conforms to a predetermined condition to determine whether the result of the examining process is correct or incorrect (checksum OK, Fig. 8, element C4); and (f) in step (c), executing the second code in the second storage device to operate the computer system after the first storage device transfers the command to the second storage device (BIOS must be running to load OS, Fig. 8, elements C8).

6. With regards to claim 3, Ishii teaches (g) in step (e), recording the predetermined instruction of the second code into the register and then checking whether the predetermined instruction conforms to the predetermined condition to determine whether the result of the examining process is correct or incorrect (checksum OK, second code must be in register to be read for basic comparison operations, Fig. 8, element C4).

7. With regards to claim 5, Ishii teaches (h) in step (b), executing the examining process when a predetermined command of the first code is executed (Fig. 8, elements C3-4); and (i) in step (d), executing a re-boot process when the result of the examining process is incorrect (Fig. 8-9, elements C9-10 and D1-5).

8. With regards to claim 7, Ishii teaches the second storage device is a random access storage device (RAM) (column 7, lines 20-30), and the second code is a basic input output system or an operating system of the computer system (load OS, Fig. 8, element C8).

9. With regards to claim 8, Ishii teaches the computer system is an information appliance (Fig. 1).

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,835,761 to Ishii et al. in further view of U.S. Patent 5,838,896 to Han et al.

12. With regards to claim 4, while Ishii does not teach comparing instructions, Han teaches comparing is a first instruction to a second instruction. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the instruction checking of Han with the BIOS load checking system of Ishii in order to prevent system malfunctions due to the loading of improper instructions.

13. With regards to claim 6, while Ishii does not teach explicitly teach the BIOS being stored in a read-only storage device (ROM), the storing a BIOS in a ROM is notoriously well known in the art. Official Notice is hereby so given.

14. Claims 24-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,835,761 to Ishii et al. in further view of the Applicant Admitted Prior Art (AAPA).

15. With regards to claim 24, Ishii teaches (a) executing the first code in the first storage device (Fig. 8, element C2); (b) after proceeding with step (a), executing an examining process before the first storage device transfers the command to the second storage device (Fig. 8, element C4); (c) after proceeding with step (b), the first storage device transferring the command to the second storage device to operate the computer system when a result of the examining

process is correct (Fig. 8, element C5); and (d) after proceeding with step (b), the first storage device not transferring or failing the command to the second storage device when the result of the examining process is incorrect (Fig. 8, elements C9). Ishii fails to storing a second code in the second storage device for indicating a state of the computer system before entering into standby mode; the computer system entering into standby mode and providing power to the second storage device for maintaining the second code in the second storage device; executing the first code in the first storage device in response to a request to exit the standby mode, but the AAPA teaches that it was well known in the art to used suspend to RAM and BIOS reloading. It would have been obvious to one of ordinary skill in the art at the time of invention to combine the STR and BIOS reload of the AAPA with the error checking of Ishii in order to ensure a proper boot up procedure.

16. With regards to claim 25, Ishii teaches (g) in step (d), examining whether a predetermined instruction of the second code conforms to a predetermined condition to determine whether the result of the examining process is correct or incorrect; and (h) in step (e), executing the second code in the second storage device to operate the computer system after the first storage device transfers the command to the second storage device (column 12, line 49, through column 13, line 8).

17. With regards to claim 26, Ishii teaches (i) in step (g), recording the predetermined instruction of the second code into the register and then checking whether the predetermined instruction conforms to the predetermined condition to determine whether the result of the examining process is correct or incorrect (column 12, line 49, through column 13, line 8).

18. With regards to claim 27, Ishii teaches the predetermined instruction is a first instruction of the second code (column 12, line 49, through column 13, line 8).

19. With regards to claim 28, (j) in step (d), executing the examining process when a predetermined command of the first code is executed; and (k) in step (f), executing a re-boot process or a debug process when the result of the examining process is incorrect.

20. With regards to claim 29, while Ishii does not teach explicitly teach the BIOS being stored in a read-only storage device (ROM), the storing a BIOS in a ROM is notoriously well known in the art. Official Notice is hereby so given.

21. With regards to claim 30, Ishii teaches the second storage device is a random access storage device (RAM) (column 7, lines 20-30), and the second code is a basic input output system or an operating system of the computer system (load OS, Fig. 8, element C8).

22. With regards to claim 31, Ishii teaches the computer system is an information appliance (Fig. 1).

Conclusion

23. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joshua D. Schneider whose telephone number is (571) 272-4158. The examiner can normally be reached on M-F, 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on (571) 272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JDS

KIM HUYNH
SUPERVISORY PATENT EXAMINER

10/17/06